In the Claims:

Please amend claims 2-5, 7, 8, 11, 13-16, 18-21, 31 and 32. Please cancel claims 1, 9, 12, 20 and 23-30. Please add new claims 33-48.

The claims are as follows:

1. (Canceled)

2. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein said repair processor is adapted to permanently disable said repairable element and replace said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

3. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

4. (Currently Amended) ~~The integrated circuit of claim 1,~~ An integrated circuit, comprising:

a pulse generator coupled to a cycle counter;

one or more repairable circuit elements;

a repair processor coupled to said cycle counter and adapted to repair a repairable circuit element of said one or more circuit elements before both (i) said repairable circuit element fails and (ii) when said cycle counter reaches a pre-determined count of pulses generated by said pulse generator; and

~~further including~~ a memory circuit adapted to store a cycle count of a number of cycles counted since an initial power up and to resume counting from said stored cycle count after a power down/power up cycle of said integrated circuit.

5. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein:

said cycle counter is adapted to generate a trigger signal when said predetermined cycle count is reached; and

said repair processor is adapted to receive said trigger signal and affect a repair of said repairable circuit element when said trigger signal is received.

6. (Original) The integrated circuit of claim 5, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

7. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, capacitor, an inductor and a wire.

8. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor is adapted to program a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

9. (Canceled)

10. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein said repair processor is adapted to perform multiple repairs by repairing previously repaired repairable circuit elements.

11. (Currently Amended) ~~The integrated circuit of claim 1, further including:~~ An integrated circuit, comprising:

a pulse generator coupled to a cycle counter;

one or more repairable circuit elements;

a repair processor coupled to said cycle counter and adapted to repair a repairable circuit element of said one or more circuit elements before both (i) said repairable circuit element fails and (ii) when said cycle counter reaches a pre-determined count of pulses generated by said pulse generator;

a redundant cycle counter; and

wherein said repair processor is adapted to replace said cycle counter with said redundant cycle counter when said cycle counter reaches a fixed cycle count.

12. (Canceled)

13. (Currently Amended) The method of claim [[12]] 15, wherein said step (e) includes permanently disabling said repairable element and replacing said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

14. (Currently Amended) The method of claim [[12]] 15, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

15. (Previously Presented) ~~The method of claim 12, further including:~~ A method of preemptively repairing an integrated circuit, comprising:

(a) providing a pulse generated for generating a pulsed signal;

(b) providing a cycle counter for counting cycles of said pulsed signal;

(c) providing one or more repairable circuit elements;

(d) providing a repair processor for repairing a repairable circuit element of said one or more repairable circuit elements when said cycle counter reaches a pre-determined cycle count;

(e) repairing said repairable circuit element before both (i) said repairable circuit element fails and (ii) when said cycle counter reaches said pre-determined cycle count; and

(f) storing a cycle count of a number of cycles counted since an initial power up in a memory circuit and resuming counting from said stored cycle count after a power down/power up cycle of said integrated circuit.

16. (Currently Amended) The method of claim [[12]] 15, further including:

said cycle counter generating a trigger signal when said predetermined cycle count is reached; and

said repair processor is receiving said trigger signal and repairing said repairable circuit element when said trigger signal is received.

17. (Original) The method of claim 16, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

18. (Currently Amended) The method of claim [[12]] 15, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a capacitor, an inductor and a wire.

19. (Currently Amended) The method of claim [[12]] 15, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor programs a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

20. (Canceled)

21. (Currently Amended) The method of claim [[12]] 15, further including said repair processor performing multiple repairs by repairing previously repaired repairable circuit elements.

22. (Original) ~~The method of claim 12, further including:~~ A method of preemptively repairing an integrated circuit, comprising:

(a) providing a pulse generated for generating a pulsed signal;

(b) providing a cycle counter for counting cycles of said pulsed signal;

(c) providing one or more repairable circuit elements;

(d) providing a repair processor for repairing a repairable circuit element of said one or more repairable circuit elements when said cycle counter reaches a pre-determined cycle count;

(e) repairing said repairable circuit element before both (i) said repairable circuit element fails and (ii) when said cycle counter reaches said pre-determined cycle count;

(f) providing a redundant cycle counter; and

(g) said repair processor automatically replacing said cycle counter with said redundant cycle counter when said cycle counter reaches a fixed cycle count.

23-30 (Canceled)

31. (Currently Amended) The integrated circuit of claim [[1]] 4, wherein:

said cycle counter is adapted to generate a signal encoding what fraction of said predetermined cycle count is reached; and

said repair processor is adapted to receive said signal and affect a repair of said repairable circuit element when said fraction of said predetermined cycle count is 1.

32. (Currently Amended) The integrated circuit of claim [[1]] 4, further including:

said cycle counter generating a signal encoding what fraction of said predetermined cycle count is reached; and

said repair processor receiving said signal and repairing said repairable circuit element when said signal encodes a fraction of 1.

33. (New) The integrated circuit of claim 11, wherein said repair processor is adapted to permanently disable said repairable element and replace said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

34. (New) The integrated circuit of claim 11, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

35. (New) The integrated circuit of claim 11, wherein:

said cycle counter is adapted to generate a trigger signal when said predetermined cycle count is reached; and

said repair processor is adapted to receive said trigger signal and affect a repair of said repairable circuit element when said trigger signal is received.

36. (New) The integrated circuit of claim 35, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

37. (New) The integrated circuit of claim 11, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, capacitor, an inductor and a wire.

38. (New) The integrated circuit of claim 11, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor is adapted to program

a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

39. (New) The integrated circuit of claim 11, wherein said repair processor is adapted to perform multiple repairs by repairing previously repaired repairable circuit elements.

40. (New) The integrated circuit of claim 11, wherein:

said cycle counter is adapted to generate a signal encoding what fraction of said predetermined cycle count is reached; and

said repair processor is adapted to receive said signal and affect a repair of said repairable circuit element when said fraction of said predetermined cycle count is 1.

41. (New) The integrated circuit of claim 11, further including:

said cycle counter generating a signal encoding what fraction of said predetermined cycle count is reached; and

said repair processor receiving said signal and repairing said repairable circuit element when said signal encodes a fraction of 1.

41. (New) The method of claim 22, wherein said step (e) includes

permanently disabling said repairable element and replacing said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

42. (New) The method of claim 22, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

43. (New) The method of claim 22, further including:

said cycle counter generating a trigger signal when said predetermined cycle count is reached; and

said repair processor is receiving said trigger signal and repairing said repairable circuit element when said trigger signal is received.

44. (New) The method of claim 43, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

45. (New) The method of claim 22, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a capacitor, an inductor and a wire.

46. (New) The method of claim 22, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor programs a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

48. (New) The method of claim 22, further including said repair processor performing multiple repairs by repairing previously repaired repairable circuit elements.